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Modified CMOS Positive Current Conveyor Based True RC Sinusoidal Oscillator

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***Abstract*—In this paper a modified CMOS positive second-generation current conveyor (CCII+) based resistance-capacitance (RC) Sinusoidal Oscillator operating over a wide frequency range is described. The proposed circuit consists of two CCII+, two buffers, four resistors and two capacitors. The oscillation conditions and the frequency of oscillations can be adjusted independently by two control resistors. Though the CCII's are available from commercial monolithic IC's viz. AD 844, PA 630, PA 630A and CCII01, but user doesn't have the access to control high frequency response, linear current gain, large output impedance, current biasing etc, in the basic internal circuit. The designed RC oscillator is desirable for VLSI realization. The power supply voltage used in the circuit were balanced and adjusted to Vdd = + 2.5V and VSS = -2.5 V. The output waveforms presented and the results discussed in the paper are the simulated outcomes of the proposed circuit, carried out using CADENCE and OrCAD Version-10 software.**

***Index Terms*—Frequency spectrum, Millers Compensation Capacitor, Op. Amp., Positive Current Conveyor.**

I. Introduction

An oscillator enjoys the same status in the domain of electrical and electronics engineering as do wheels in the mechanical engineering. Sinusoidal Oscillators of variable frequency find wide range of applications in instrumentation & measuring systems, communication, control systems and signal processing. For the implementation of RC (resistance–capacitance) sinusoidal oscillator the voltage-mode operational amplifier circuits have been shown to be very commonly used due to its simplicity in design only, but at the same time it suffers a number of disadvantages. The first is that in voltage mode the circuit's parasitic capacitances create dominant poles at relative low frequencies, which limits the bandwidth. The second is the dynamic range of operation dictated by the frequency-dependent gain of op-amp. The third is the difficulty to change the frequency of oscillation independent of the necessary and sufficient condition required to sustain the oscillations. On the other hand the current-mode op amp circuits like CCII+, has shown to offer improved performance over the conventional op-amp-based oscillators.

It has low node impedances and the small voltage swings. Thus the time constant effect is minimal. Hence the slew rate is sufficiently high. They are well suited to work at higher frequencies. It has larger dynamic range and wider bandwidth. Furthermore they are also suitable for integration with CMOS technology and thus become more and more attractive in electronic circuit design. Hence in recent years the current-mode circuits are most widely used instead of their voltage-mode counter parts and it has shown that the CCII+ is very useful as an analogue building block and receiving much attention in oscillator design [1,2,3]. The implementation of Integrated Circuit (IC), technology has gone extremely advanced and the plus-type CCIIs are now available from commercial monolithic IC's, like PA 630, PA630A (Phototronics), AD 844 (Analog Devices) and CCII01 (LPT Electronics Ltd) [4].

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II. Circuit Description and Simulation

Here we have developed and designed a novel second generation current conveyor CCII+) and has used it in the form of an integrable block as shown in Figure1. The same is used to realize RC Sinusoidal Oscillator to generate the oscillations over a wide range of high frequency.

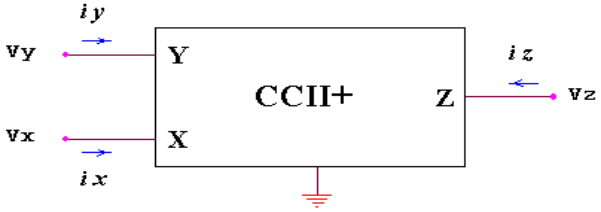

Fig. 1 The Basic CCII+ Block

The terminal characteristics of CCII+ can be defined by the following matrix equation:

$$\begin{bmatrix} i_y \\ v_x \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & +1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_Z \end{bmatrix} \quad \text{.....(1)}$$

Thus an ideal CCI has the following terminal characteristics

$i_y = 0$, $v_x = v_y$, and $i_z = + i_x$.

The output current iZ, thus, depends only on the input current ix at terminal X (Fig.1) which may be injected directly at X, or it may be produced by the copy of the input voltage Vy, from terminal Y, acting across the impedance connected at X. The proposed CMOS CCII+ based circuit diagram is shown in figure 2 which has further been implemented for simulation on CADANCE software using two CCII+ and two buffers as depicted in figure 3.

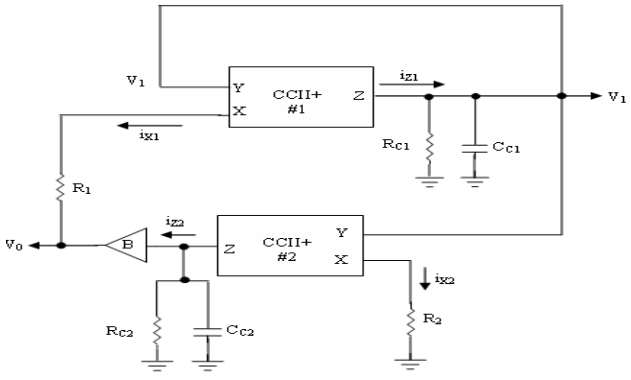

Fig. 2 Proposed CMOS CCII+ Sinusoidal Oscillator

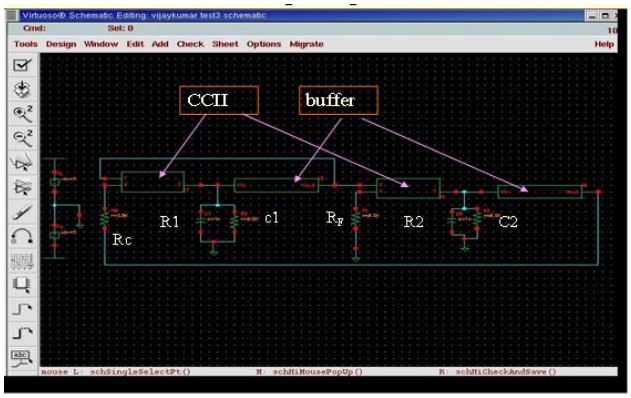

Fig. 3 The Proposed Model of Oscillator which is used for Simulation on CADANCE software.

The proposed CMOS RC sinusoidal oscillator was also produced with PSPICE simulator integrated with OrCAD V.10 as shown in figure 3. The dc voltage used were ± 2.5 V.

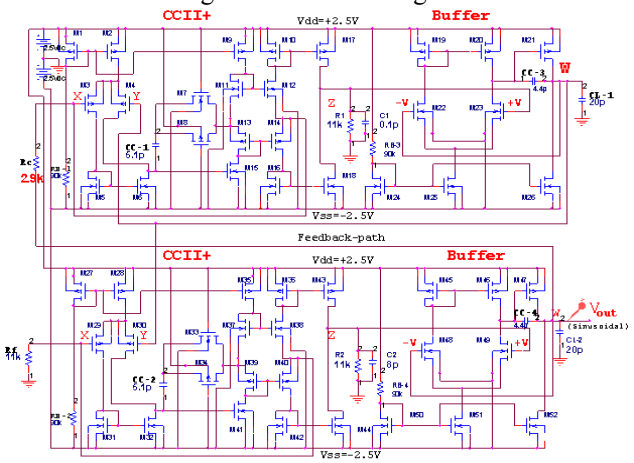

Fig. 4 The Proposed Circuit of RC Sinusoidal Oscillator using OrCAD Software.

During simulation, first we have considered the case of growing (at RC = 3.2 KΩ) , sustaining (RC = 3.79 KΩ) and dying (RC = 4.6 KΩ) oscillations as shown in figure 4. The values of other components used in the circuit have the values: R1 = R2 = RF =11 KΩ, C1 = 0.1 pF, C2 = 8 pF, the value of Millers compensation capacitor (CM) is 5.1 pF. The frequency generated was 120 KHz. The frequency spectrum of the waveform is shown in figure 5.

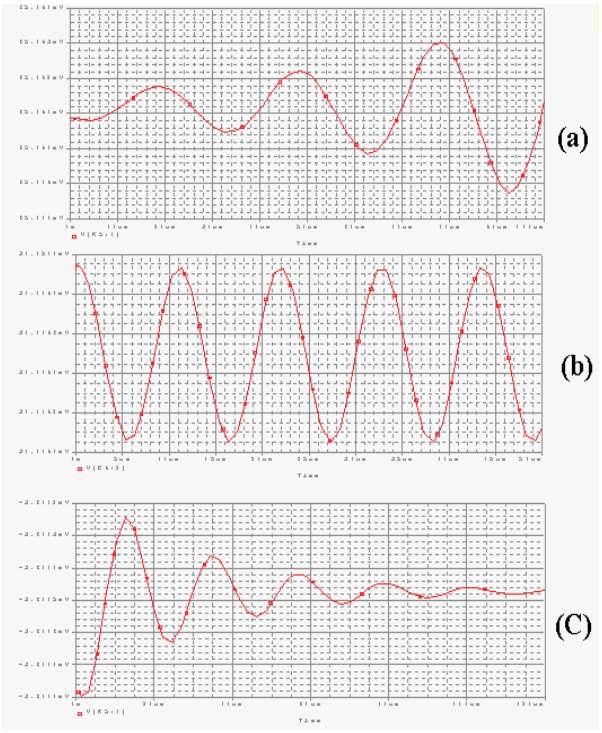

Fig. 5 Waveform at 120 KHz Frequency

(a) Growing Oscillations (b) Sustaining Oscillations
(c) Dying Oscillations

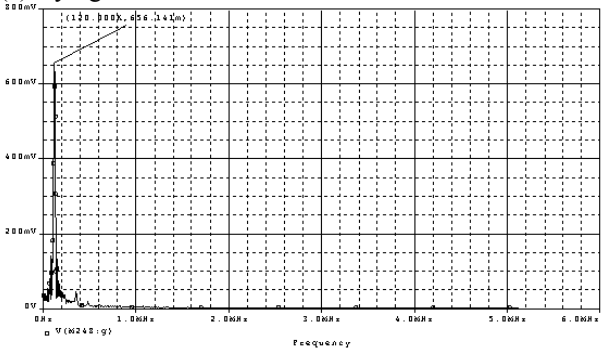

Fig. 6 Frequency Spectrum of the Waveform at 120 KHz

III. Optimization of Experimental Results

As the idea of working research was to optimize the circuit for stability and to achieve the highest frequency possible by varying the value of components like coupling capacitors, load capacitors, terminal impedances, feedback register etc. The same has been carried out in the following steps case wise.

Case-1:

R1 = R2 = 14KΩ, RF =10KΩ, RC =3.1 KΩ, C1= 0.1 pF, C2=0.3 pF, CC-1 = 0.1 pF, CC-2= 0.1 pF, CC-3=0.022 pF, CC-4 =0.022 pF, CL-1= 0.1 pF, CL-2=0.1 pF.

Results:

Delay in start of oscillation = 145 ns (Fig.7)
Frequency achieved = 32.000 MHz (Fig.8)
Amplitude achieved = 947.064 mV (Fig.8)

The output voltage Vout with time, at frequency 32.000 MHz is shown in figure 6 and the corresponding frequency spectrum of the same waveform is shown in figure 7.

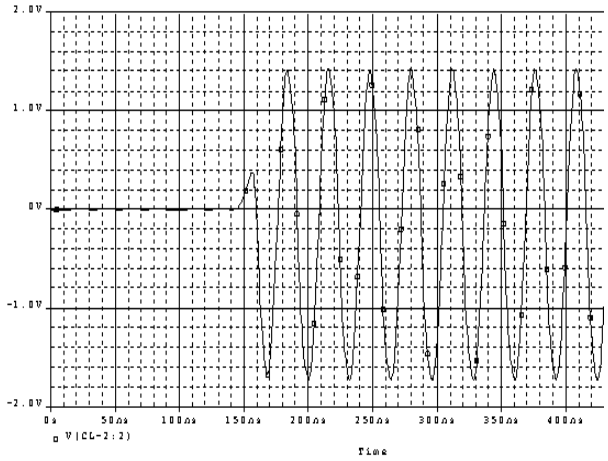

Fig. 7 The Simulated Output Waveform at 32.000 MHz.

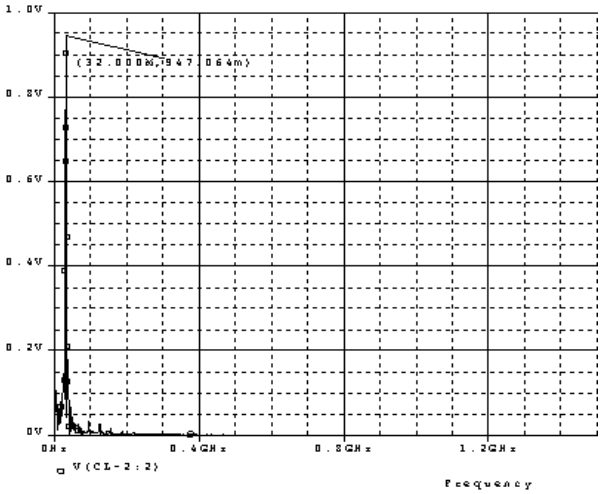

Fig. 8 The frequency spectrum of the waveform in Fig.7

Caes-2:

R1 = R2 = RF = 14KΩ, RC =3.4 KΩ, C1= CC-1 = CC-2= CL-1= CL-2= C2 = CC-3= CC-4 == 0.00001pF.

Results:

Delay in start of oscillation = 50 ns (Fig.9)
Frequency achieved = 80.000 MHz (Fig.10)
Amplitude achieved = 697.856 mV (Fig.10)

The output voltage Vout with time, at frequency 80.000 MHz is shown in figure 8 and the corresponding frequency spectrum of the same waveform is shown in figure 9.

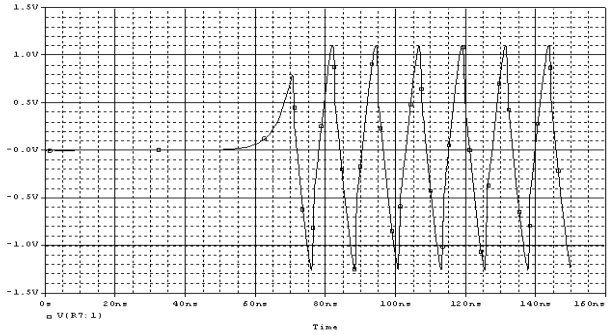

Fig. 9 The Simulated Output Waveform at 80.000 MHz.

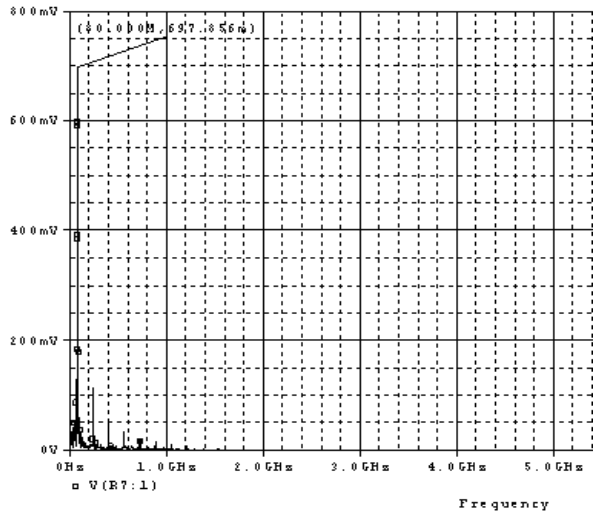

Fig. 10 The frequency spectrum of the waveform in Fig.9

Case-3:

R1 = R2 = RF = 14KΩ, RC =3 Ω, C1= CC-1 = CC-2= CL-1= CL-2= 0.00001pF, C2 = 0.2 pF, CC-3= CC-4 = 0.0000022 pF.

Results:

Delay in start of oscillation=117.64 ns (Fig.11)
Frequency achieved = 94.000 MHz (Fig.12)
Amplitude achieved = 669.13 mV (Fig.12)

The output voltage Vout with time, at frequency 94.000 MHz is shown in figure 10 and the corresponding frequency spectrum of the same waveform is shown in figure 11.

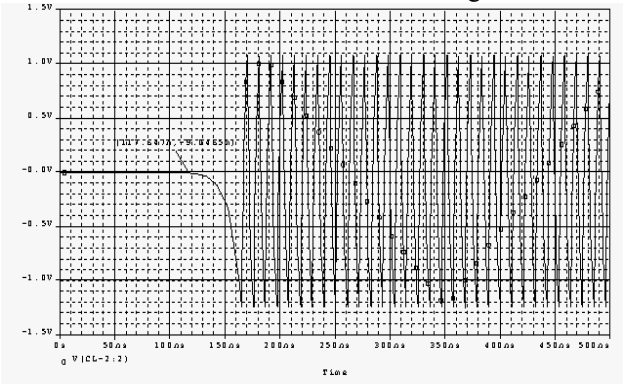

Fig. 11 The Simulated Output Waveform at 94.000 MHz

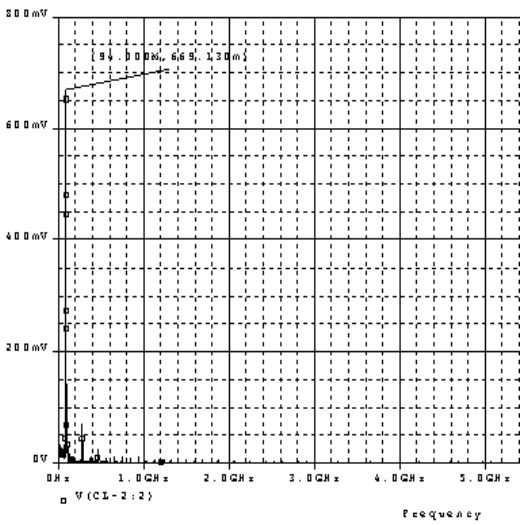

Fig. 12 The frequency spectrum of the waveform in Fig.11

IV. Conclusion and Futre Scope

A proposed modified CMOS CCII+ based Sinusoidal Oscillator has been described and simulated up to a maximum frequency of 94 MHz. The circuit allows independent control of the oscillation conditions and oscillation frequencies which are controllable with the help of resistors RF and a few capacitors i.e. C1, C2, CC1, CC2, CC3, CC4, CL1 and CL2 in combination. The main advantage of the circuit is the use of CMOS CCII+ instead of conventional operational amplifiers. With the present trend towards the design of current-mode circuits and because the ground capacitors structures are compatible with the CMOS technology, the proposed configuration will be more suitable for adaption to monolithic IC form in future. This is desirable for VLSI realization. The circuit shows that the experimental results conform well with the simulation and theoretical conclusions.

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